

Non-volatile molecular memory elements based on ambipolar nanotube field effect transistors

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Abstract

We have fabricated air-stable n-type, ambipolar carbon nanotube field effect transistors (CNFETs), and used them in nanoscale memory cells. N-type transistors are achieved by annealing of nanotubes in hydrogen gas and contacting them by cobalt electrodes. Scanning gate microscopy reveals that the bulk response of these devices is similar to gold-contacted p-CNFETs, confirming that Schottky barrier formation at the contact interface determines accessibility of electron and hole transport regimes. The transfer characteristics and Coulomb Blockade (CB) spectroscopy in ambipolar devices show strongly enhanced gate coupling, most likely due to reduction of defect density at the silicon/silicon-dioxide interface during hydrogen anneal. The CB data in the “on”-state indicates that these CNFETs are nearly ballistic conductors at high electrostatic doping. Due to their nanoscale capacitance, CNFETs are extremely sensitive to presence of individual charge around the channel. We demonstrate that this property can be harnessed to construct data storage elements that operate at the few-electron level.

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Since the first demonstration of molecular carbon nanotube field effect transistor (CNFET) [1,2] just four years ago, exploration of the potential of this system for use in functional electronic devices has proceeded at a rapid pace. Typical transistor circuits are p-type i.e., holes are majority carriers, an effect originally ascribed to exposure to ambient gas [3]. Recently, scanning gate microscopy (SGM) [4] as well as transport experiments [5,6] have shown that the charge transport is influenced by formation of Schottky barriers at the nanotube-electrode contact. More importantly, Derycke et al. [6,7] can adjust the Schottky barrier height using a combination of annealing and oxygen exposure, which allows them to continuously tune from p-type to ambipolar to n-type, i.e. electron transport. These advances have led to integration of CNFETs into the first molecular logic gates. [6,8,9] To date however, all n-CNFETs have been enclosed for protection from oxygen: either in a vacuum chamber [10] or by a silicon-dioxide passivation layer [5] which may not be suitable for applications such as in sensor technologies.

In this Letter we demonstrate the first air stable n-type CNFET in the more traditional open geometry. SGM data reveals that bulk response of n-CNFETs is complementary to p-type CNFETs with gold electrodes, verifying that carrier type is a function of the barrier at the contact interface. Favorable Fermi level alignment enables observation of ambipolar transport in these devices. [5] Our CNFETs show drastic increase in gate coupling, which we attribute to reduction trap density at Si/SiO₂ during the hydrogen anneal. For large negative gate potential (hole transport regime) CNFET forms a single quantum dot at low temperatures, suggesting that transport becomes ballistic. Finally we exploit a hysteresis phenomenon to create molecular memory cell based on a single CNFET that is stable on the scale of days at room temperature.

CNFET devices are fabricated from nanotubes grown directly on the substrate using chemical vapor deposition. [11,12] Chrome/gold alignment marks are patterned on degenerately doped p⁺⁺ Si wafers capped with 225nm of thermally grown SiO₂. Next, catalyst consisting of ethanol solution of fused alumina and ferric nitrate [13] is randomly dispersed on the substrate. Nanotubes are grown by catalytic decomposition of ethylene gas at 800°C. [12] While ethylene (2sccm) is only streamed at setpoint temperature, hydrogen (400sccm) and argon (600sccm) flow through the furnace during heating and cooling cycles. Hydrogen has a two-fold role: first, it protects nanotubes from burning by reacting with residual oxygen in the environment. Second, it prevents degradation of the substrate and keeps the trap density at Si/SiO₂ interface to a minimum. [14] We perform hydrogen anneal prior to contact fabrication in order not to influence the Schottky barrier at the CNFET-electrode interface. Following growth, nanotubes are located with respect to alignment marks, and source and drain connections are fabricated by electron beam lithography and liftoff.

Figure 1 shows current-gate voltage ($I-V_g$) transfer characteristics for devices grown during the same run, and fabricated with either chrome/gold (Cr/Au) or cobalt (Co) electrodes. A distinct difference is always observed between two sets of devices: Cr/Au-contacted CNFETs are intrinsically p-type, while Co connection yields n-type $I-V_g$ behavior (Fig. 1(a)). N-type conduction is stable under ambient conditions and observed in twelve CNFETs grown in three different runs. To further examine this issue we perform scanning gate microscopy (SGM) [15,16] on both p- and n-CNFETs (Fig. 1(b)-(e)). The conductance of p-CNFETs is suppressed at localized scattering sites within the nanotube by a positive SGM tip voltage, V_t (Fig. 1(c)). In contrast, a negative V_t only has an effect at the nanotube-metal junc-

tion, where it enhances device conductance by increasing the transparency of the reverse biased Schottky barrier at the source electrode. [4] SGM reveals that the response of n-type, Co-contacted transistors to local gating is complementary to that of p-CNFETs: Fig. 1(e) shows that scattering sites along the nanotube are imaged for $V_t < 0$. The Schottky barrier at the nanotube-cobalt interface is weaker than in the case of Cr/Au electrodes (data not shown). Our findings demonstrate the possibility of open-geometry air stable n-CNFET, and support previous results [5] that device switching is influenced by the precise nature of the nanotube-metal contact. Moreover, these data add to the mounting evidence [6] that suggests that hole density induced by charge transfer between tube and adsorbed gases in the ambient is not large enough to dominate device behavior under all circumstances.

The observed p- to n-type conversion must be understood in terms of precise control of the Schottky barrier at the device interface depending on the contact scheme [6]. Work function difference alone can not account from the observed shift since those of chrome (4.5eV) and cobalt (5.1eV) are both higher than the nanotube workfunction (4.5eV). [17] In addition, previously fabricated Co-CNFET devices are found to be p-type. [18] Some differences between two types of devices are evident: First, contacts between metallic nanotubes and cobalt have near-perfect transparency (as high as 98%), while Cr/Au contacts have transmission below 80%. [19] Second, they behave differently in the electron accumulation regime. Cr/Au contacts lead to a sizeable Schottky barrier [4,5] for electron injection at the contacts. This occasionally leads to production of a nanoscale quantum dot at the end of the nanotube. [20] We do not observe this effect in n-type devices, suggesting a lower barrier height for the cobalt-CNFET system, consistent with SGM data. It is clear that two contact schemes are not equally affected by processing and environmental conditions. This presents an opportunity to differentiate the contributions of different factors to the Schottky barrier height in nanotube systems, which should allow individual control over device properties.

Figure 2 shows $I - V_g$ characteristics at fixed bias (V_{ds}) for an $L = 800\text{nm}$ long, Co-contacted CNFET. At $V_g=0$, electrons are the majority carriers, and the conductance decreases as the gate voltage is made negative. Surprisingly, at more negative gate voltage, the conductance increases again, a signature of room temperature inversion to hole conduction in the device. Ambipolar transport has been observed starting from a traditional p-CNFET in our group and others. [5,19,20] In our samples, the resistance in inversion is typically five times larger than in accumulation. Since device conductance, which is less influenced by bulk scattering (see Coulomb blockade data below) than tunnelling through the Schottky barrier at the source electrode [4], is similar in two transport regimes so are the barriers for the two carrier types. Cobalt-contacted CNFETs also show excellent switching characteristics for both electrons and holes. From Fig. 2(b) we extract transconductances of $2\mu\text{A/V}$ and $3\mu\text{A/V}$ at $V = 1\text{V}$ for holes and electrons, respectively, an order of magnitude better than previously reported in solid-state devices. Using $dI/dV_g = \mu C_g V/L^2$ [21], we infer a high carrier mobility on the order of $\mu = 400\text{cm}^2/\text{V-s}$ even at large 1V source-drain potential. As shown below, the transport in CNFETs is not limited by scattering in the nanotube bulk, and so the computed mobility is an “effective” quantity that characterizes device performance and only a lower bound on the intrinsic mobility of the semiconducting nanotubes. Lastly, our devices exhibit voltage gain ($\Delta V_{ds}/\Delta V_g$, at $P = 0.5\mu\text{W}$; data not shown) between 2 and 3 in either regime, surpassed only by devices with electrolyte [22] and very thin aluminum oxide dielectric layers. [8] Voltage gains larger than 1 are required in

order to prevent signal degradation through multiple logic elements. High gain in accumulation and inversion should enable integration of solid-state, complementary logic elements on an individual CNFET. [6]

Low bias $I - V_g$ data (Fig. 2(a)) shows that the nanotube band gap corresponds to $\delta V_g = 2.0\text{V}$. Based on the nanotube diameter, measured by AFM, we estimate the band gap to be $E_G = 0.6\text{eV}$. The ratio $\alpha_g = E_G/\delta V_g = C_g/C$ is the electrostatic “lever arm” of the gate (here C_g and C are the gate capacitance and total capacitance of the CNFET, respectively). Our measured value $\alpha_g = 0.33$ is an order of magnitude larger than that previously observed in CNFET devices. [23] We confirm this measurement of α_g with Coulomb blockade (CB) data [24] from which C_g/C can be calculated. Figure 2(d) shows the differential conductance of the *same* CNFET as a function of the bias and gate voltages at $T = 5\text{K}$ in the hole accumulation regime. Current through the device is blocked within the black diamonds in the $V - V_g$ plane. Extraordinarily regular size and spacing of Coulomb diamonds indicates that the CNFET forms a single quantum dot, a signature of *ballistic transport* [25] within the semiconducting nanotube on the scale of 800nm at sufficient electrostatic doping. This is in contrast to early proposals of diffusive transport in CNFETs. [2,23] We find the capacitive lever arm of the gate by comparing the charging energy of the nanotube to the period of Coulomb oscillations: $\alpha_g = 6\text{mV}/15\text{mV} = 0.4$, close to the value derived from room temperature data. We consistently find gate lever arms of $0.2 - 0.4$, strong evidence that annealing of the oxide film in hydrogen and the associated reduction in trap density improves gating action and ambipolar transport in nanotube devices. Extremely good transconductance and subthreshold swing values compare favorably to ambipolar CNFETs fabricated using two orders of magnitude thinner dielectric layers [8] or electrolytic gates [22].

We quantitatively explain the enhanced gate coupling as due to improvement of the gate oxide layer through the hydrogen anneal. Silicon dioxide has interface and bulk (dangling bond) traps whose charge state changes with gate voltage (Fig. 2(c)). High quality as-grown oxide films have trap densities $D_{it} \sim 5 \times 10^{11}/\text{cm}^2\text{-eV}$ and $N_{ot} \sim 5 \times 10^{11}/\text{cm}^2$ for interface traps at midgap and oxide traps, respectively. [14] Interface traps are populated continuously as the gate voltage is tuned, while oxide traps are charged only with injection at gate fields above $3 \times 10^5\text{V/cm}$. Here we focus on interface traps; we discuss bulk oxide traps in the context of large gate fields in the next paragraph. The backgate voltage is screened effectively by traps within a $L \times (2\pi h)$ rectangular cutout of the outer cylinder in the coaxial cable approximation for CNFET capacitance (L is the device length, h the dielectric thickness [26]). This implies that in the area beneath the CNFET there are $7000/\text{eV-}\mu\text{m}$ interface traps, much larger than the total device capacitance, $C = 130\text{e}/\text{V-}\mu\text{m}$. The lever arm is approximately the ratio between the self capacitance and the trap density: $\alpha_g \sim 130/7000 = 0.018$, a value similar to that observed by other groups. [25] Our measurement $\alpha_g = 0.4$ indicates that the interface trap density is reduced by a factor of 50 to $D_{it} \sim 2 \times 10^{10}/\text{cm}^2\text{-eV}$, which is consistent with expectations for the anneal conditions. [14]

Figure 3(a)-(c) compares room temperature $I - V_g$ curves of an ambipolar, Co-contacted CNFET for different V_g ranges. There is reproducible hysteresis in the $I - V_g$ curves that becomes larger as the range of V_g is increased, indicating that it originates from avalanche injection into bulk oxide traps. Hysteresis can become so large that the device varies between depletion mode (normally-“on” at $V_g = 0$) and enhancement mode (normally-“off”)

behavior. We determine the location and sign of trapped charges by comparing the direction of the hysteresis to the avalanching field. After a sweep to positive V_g , the CNFET threshold voltage moves toward more *positive* gate values indicating injection of *negative* charges into oxide traps. Traps are populated by electrons injected from the CNFET channel, where the electric field is highest due to the cylindrical device geometry. These charged traps are near the device [27], perhaps the same scattering sites imaged in SGM (Fig. 1(c) and (e)).

The hysteresis allows the device to function as a non-volatile memory cell, similar in operation to electrically erasable, programmable read-only memories (EEPROMs [28]). To read out the memory, a $1\text{M}\Omega$ load resistor is added to create a voltage divider circuit (Fig. 3(e), inset). Read ($V_{in} = 0$) and write ($V_{in} = +20\text{V}$ or -20V) are applied to the input (backgate) terminal. Logical “1” (“0”) is defined as $V_{out} = 1\text{V}$ (0V). To write a “1” (“0”) to the memory cell, V_{in} is switched rapidly to -20V ($+20\text{V}$) and back to 0, so the CNFET is “on” (“off”) at the read voltage (c.f. Fig. 3(c)). Figure 3(e) shows the memory cell output as a function of time while a series of data bits is written. Irregular sequence of bit values and writing times is used to demonstrate stability of the memory cell. The CNFET-based memory is non-volatile at room temperature, with bit storage times of at least 16 hours. The device read/write speed is limited by trap charging times, which are much shorter than the 100Hz pulses used here. The number of occupied trap charges is estimated from the threshold voltage shift and an effective capacitance: $\Delta Q_{ot} = C_{\text{eff}}\Delta V_T$, where C_{eff} is related to the active oxide region for data storage, located near the Schottky barriers (of order 20nm width [29]). The bit is stored in no more than $2e$, $70e$ and $200e$ charges (for Fig. 3(a)-(c), respectively), quantitatively similar to floating gate single-electron memory devices based on conventional silicon transistors. [30] More controllable, single-electron data storage may be achieved by intentional fabrication of charge storage sites in the active device region.

In conclusion, air-stable and intrinsic n-type, ambipolar CNFETs [5] can be fabricated by controlling the Schottky barrier [4]. Excellent switching characteristics are achieved when the gate oxide is subject to hydrogen anneal. Our observation of an order of magnitude improvement in gate lever arm is directly verified using Coulomb blockade data in the strong inversion regime. The existence of a single quantum dot within the nanotube at low temperatures suggests that at high doping levels semiconducting nanotubes, like their metallic counterparts, are ballistic conductors on the $1\mu\text{m}$ scale. Finally, we have harnessed charge injection into the oxide at large gate voltage to construct a nanotube-based molecular memory cell with data storage nearly at the single-electron level. [31]

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- [26] CNFET capacitance per unit length is derived from the cylindrical geometry: $C/L = 2\pi\epsilon\epsilon_o/\ln(2h/r)$ or $21\text{aF}/\mu\text{m} = 130e/\mu\text{m-V}$ for our devices.
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- [31] During preparation of this article, we became aware of similar research done by M. S. Fuhrer and collaborators. They have observed an even higher “effective” mobility than we have, in agreement with our claim of near-ballistic transport in these devices. Additionally, they have observed the memory effect we investigated.

FIGURES

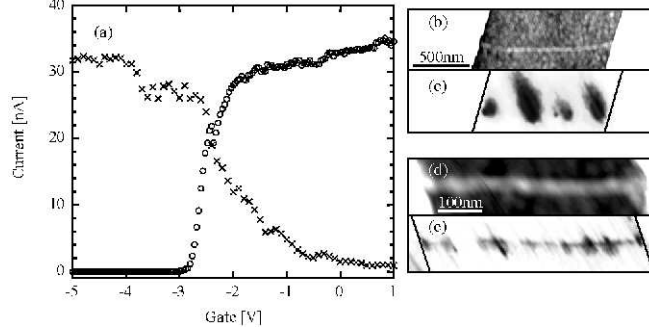


FIG. 1. Complementary CNFETs: (a) Ambient $I - V_g$ curves for Cr/Au-contacted p-type CNFET (crosses) and Co-contacted n-type CNFET (circles) (bias voltage $V_{ds} = 10\text{mV}$). “On”-state resistance is $300\text{k}\Omega$ and switching ratio exceeds 10^5 . (b)-(c) Topographic AFM and SGM scans for a CNFET with Cr/Au electrodes. SGM ($V_t = +2\text{V}$, $V_{ds} = 50\text{mV}$) shows a series of well-localized, gateable regions along the CNFET. Grayscale in (c) represents transport currents between 0 (black) and 400nA (white). (d)-(e) Corresponding data for a Co-contacted CNFET in the ambient. SGM ($V_t = -1.2\text{V}$, $V_{ds} = 200\text{mV}$) shows complementary gateable regions sensitive to the negative tip voltage. The grayscale in (e): 0 (black) to 250nA (white).

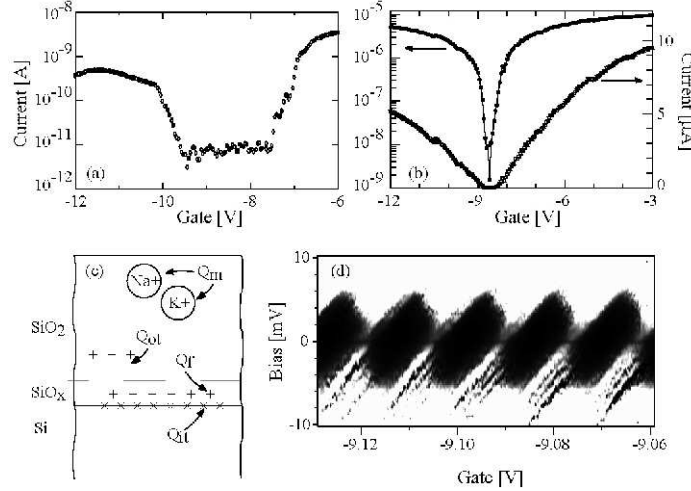


FIG. 2. (a) $I - V_g$ characteristic ($V_{ds} = 0.5\text{mV}$) shows ambipolar transistor action. (b) Same sample at $V_{ds} = 1\text{V}$ shows transconductance of approximately $3\mu\text{A/V}$ for electrons and $2\mu\text{A/V}$ for holes and subthreshold swing of 100mV/decade . (c) Schematic depicts interface (Q_{it}) and bulk (Q_{ot}) oxide traps. (d) Coulomb Blockade data for the CNFET in hole conduction regime. Uniform CB is consistent with a long mean free path in doped semiconducting nanotubes.

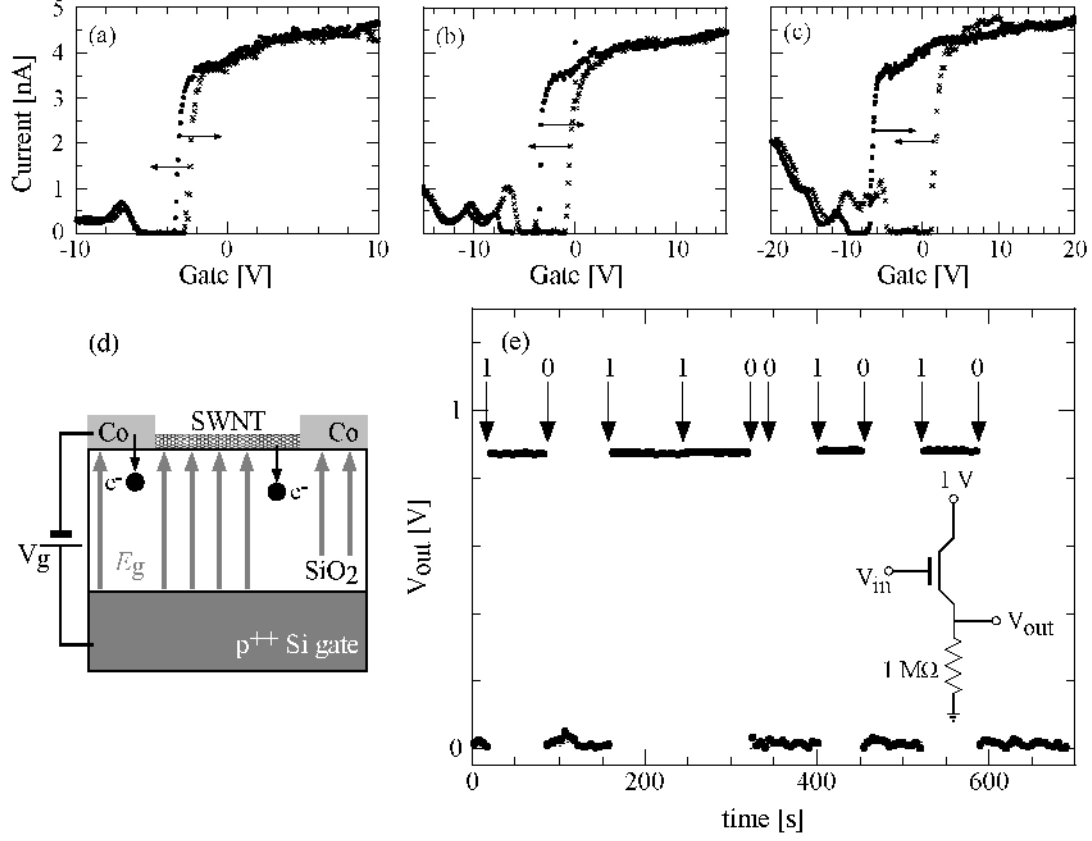


FIG. 3. (a)-(c) High vacuum $I - V_g$ data at $V_{ds} = 0.5\text{mV}$. Device hysteresis increases steadily with increasing V_g due to avalanche charge injection into bulk oxide traps. (d) Diagram of avalanche injection of electrons into bulk oxide traps from the CNFET channel. (e) Data from CNFET-based non-volatile molecular memory cell. A series of bits is written into the cell (see text) and the cell contents are continuously monitored as a voltage signal (V_{out}) in the circuit shown in the inset.

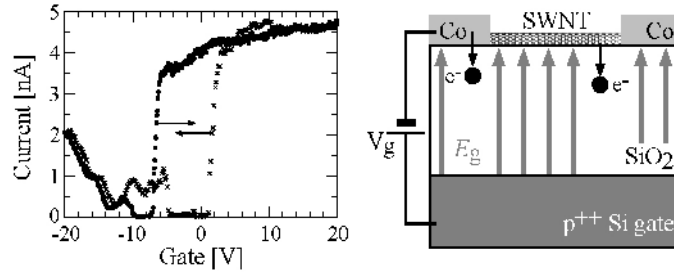


FIG. 4. Table of Contents graphic